APPARATUS AND METHOD FOR INPUT CLOCK SIGNAL DETECTION IN AN ASYNCHRONOUS TRANSFER MODE INTERFACE UNIT

Abstract of the Disclosure

In a data processing system have a master-state data processing unit and at least one slave-state data processing unit, the data processing units can be provided with an asynchronous transfer mode interface unit for transferring data cells there between. The interface unit provides and receives signals formatted in the Utopia protocol. The interface unit clock signals from an external source or from the master processing unit. To insure the integrity of the data transfer through the interface unit, a clock signal detection system is provided. When the applied clock signal is not detected, a reset signal and an interrupt signal are generated.